Memory PHYs

With their reduced power consumption and industry-leading data rates, our line-up of enhanced memory interface IP solutions support a broad range of industry standards with improved margin and flexibility.

Fully Standards-Compatible
- Compliant with the latest JEDEC and industry-standard specifications
- Support for multi-modal functionality

Enhanced Design Flexibility
- Support for multiple packaging options
- Enhanced margin and yield

Reduced Power
- Improved power efficiency
- Lower signaling and stand-by power

Improved Performance
- Increased data rates
- Improved bandwidth
- Higher capacity
Memory PHYs

Overview
From mobile to consumer to enterprise, today’s applications all continue to demand greater performance at lower power. Our family of enhanced, standards-compliant memory PHYs offer a number of compelling benefits to chip and system designers alike, including reduced power consumption, increased data rates and improved cost-effectiveness – giving designers the advantage of increased margin and flexibility.

Designed to meet the needs of a broad range of applications, our memory PHYs support multiple packaging and system configuration options to deliver enhanced usability and superior flexibility. Each PHY is part of a complete solution that includes all of the necessary components for robust operation and ease of integration. The family of solutions includes:

**PHYS:**
- HBM Gen2 PHY
- DDR4 Multi-modal PHY
- DDR4 PHY
- DDR3 PHY

**Tools:**
- LabStation™ Validation Platform
- On-chip Power Supply Noise Monitor

**Example DDRn PHY Configuration**

**Features**
- DFI and JEDEC standards compliant
- Support for multiple channel configurations
- Includes FlexPhase™ per bit deskew of data and clock signals for simplified design
- Available option with LabStation Validation Platform for enhanced bring-up and validation

**Deliverables**

**Fully characterized hard macro (GDSII)**

**Complete design views:**
- Gate-level and I/O models
- Verification test benches
- Layout abstracts (.lef)
- Timing models (.lib)

**Full documentation:**
- Datasheet
- Integration guidelines
- Package and PCB design guidelines
- ASIC/DFT manufacturing guidelines
- Test and characterization user guide
- Verilog models
- CDL netlists (.cdl)
- ATPG models
- GDSII layout
- DRC & LVS reports

**Optional design integration and bring-up services**

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